33 ~~38.~~   (Currently Amended) A computer system, comprising:

a plurality of processors, wherein the processors includes means for issuing a write address separate from data to be written to the write address; and

a shared memory connected to the plurality of processors, wherein the shared memory includes:

means for receiving a <u>first</u> write request including a <u>first</u> write address; ~~and~~

<u>means for comparing addresses in subsequent load and store requests to the first write address; and</u>

means for stalling subsequent ~~loads and stores~~ <u>load and store requests</u> to <u>a memory location in the shared memory associated with</u> the <u>first</u> write address ~~in shared memory~~ until the data ~~to be written to the write address~~ <u>associated with the first write request</u> is received and written by the shared memory.